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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/588,617	06/06/2000	Claude L. Bertin	BUR9-1999-0264-US1	1077

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EXAMINER
NGUYEN, TRUNG Q

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/588,617	BERTIN ET AL.	
	Examiner	Art Unit	
	Trung Q Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings, which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 9-10, 13-18, 21-30 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaneko et al. (U.S. 5,534,786).

Regarding claims 1-3, 30 and 32, Kaneko discloses a method for testing semiconductor components (Fig. 5) comprising a plurality of semiconductor devices (3 or A1-C3 of Fig. 4); a device carrier (6) having interconnect wiring therein sufficient for both testing and end use operation (column 3, lines 35-44); attaching semiconductor device (3) to carrier (6); dividing carrier into a plurality of components (3, 5 6 and 9 of Fig. 5); the step of installing one component on a next level of assembly without separating device from carrier (6, 7 and 8 of Fig. 5) and without separating device from carrier (Fig. 5).

Regarding claim 4, Kaneko discloses carrier comprises a printed circuit board (column 4, lines 36-40).

Regarding claims 9-10, 13-18 and 21 Kaneko discloses semiconductor devices (3) are organized in a plurality of groups on carrier (3 and 6 of Fig. 5); and testing groups of devices in parallel with a separate reader (9) for each group; a running semiconductor devices simultaneously independently of each other and single-in-line multi-chip modules assemblies (6, 7 and 8 of Fig. 5). Kaneko also discloses a step of mounting semiconductor component on a second carrier (7 and 8 of Fig. 5) wherein second carrier comprises a printed circuit board (column 4, lines 36-40).

Regarding claims 22-27, Kaneko discloses the step of encapsulating semiconductor device and carrier (3 and 6 of Fig. 5) in an encapsulant (5); identifying and repairing defective semiconductor devices (column 3, 20-45 and column 5, lines 23-32).

Regarding claims 28-29, Kaneko discloses the semiconductor devices are memory chips (column 4, line 48) and a step of testing functionality (column 5, lines 7-14).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-8, 11-12,19-20 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al. (U.S. 5,534,786) in view of Nakata (U.S. 5,945,834).

Regarding claims 5-8, 11-12, 19-20 and 31, Kaneko fails to disclose the semiconductor device comprises a plurality of leads, pads, tabs and BIST self test circuit. However, Nakata discloses a plurality of leads (15 of Fig. 6a), pads (14 of Fig. 6a); tabs (17 of Fig. 6a) for external contact between semiconductor device (12) to carrier (77 of Fig. 14b) and a plurality of BIST self test circuit for shortening a test time per chip (column 35, lines 1-6).

Therefore, at the time of the subject invention, it would have been obvious for a person of ordinary skill in the art to use a plurality of leads, pads, tabs and BIST self test circuit as taught by Nakata in the system of Kaneko because they are easy to install, convenience, great reduction of mechanism for external contact between a semiconductor device to carrier contacts, small scale, and readily availability.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. As already mentioned, there are a number of prior art references dealing with the use of device under test board and testing method; only a representative sample is cited herein.

Whetsel (U.S.6,046,600) discloses a process of testing integrated circuit dies on a wafer.

Farnworth (U.S. 5,894,218) discloses a method and apparatus for automatically positioning electronic dice within component packages.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Nguyen whose telephone number is 703-305-4925. The examiner can normally be reached on Monday through Friday, 8:30AM – 5:00PM. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached at 703- 308-1680.

3/25/02

TN
March 25, 2002

MICHAEL J. SHERRY
PRIMARY EXAMINER